Claims

1. A method for forming a semiconductor device, comprising:
forming a conductive bond pad over a semiconductor substrate;
forming a dielectric layer over the conductive bond pad;
removing portions of the dielectric layer; wherein removing portions of the first dielectric forms a plurality of support structures that overlie the conductive bond pad, and wherein removing portions of the dielectric layer exposes a portion of the conductive bond pad; and
forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts a portion of the conductive bond pad.

2. The method of claim 1, wherein the conductive bond pad comprises mostly copper.

3. The method of claim 2, further comprising forming dielectric studs within the conductive bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud.

4. The method of claim 1, wherein the dielectric layer includes a material selected from a group consisting of a nitride and a hydrogen and carbon containing silicon oxide.

5. The method of claim 1, wherein the plurality of support structures are interconnected with unremoved portions of the dielectric layer.

6. The method of claim 5, wherein forming the conductive bond pad further comprises forming the conductive bond pad over at least one

dielectric layer having a Young's modulus less than approximately 50 Giga Pascals.

7. The method of claim 5, wherein forming the conductive bond pad further comprises forming the conductive bond pad over at least one dielectric layer having low yield strength.

8. The method of claim 1, further comprising forming a barrier layer between the capping layer and the conductive bond pad.

9. The method of claim 8, wherein the barrier layer includes a material selected from a group consisting of tantalum, titanium, tungsten, and chromium.

10. The method of claim 1, wherein the conductive capping layer includes aluminum.

11. The method of claim 1, wherein the conductive capping layer includes a material selected from the group consisting of nickel and palladium.

12. A semiconductor device comprising:

a conductive bond pad over a semiconductor substrate;

a dielectric layer over the conductive bond pad;

a plurality of support structures overlying the conductive bond pad; and

a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts a portion of the conductive bond pad.

13. The semiconductor device of claim 12, wherein the conductive bond pad comprises mostly copper.

14. The semiconductor device of claim 12, further comprising a dielectric stud within the conductive bond pad, wherein the at least a portion of at least one of the plurality of support structures overlies a portion of the dielectric stud.

15. The semiconductor device of claim 12, wherein the dielectric layer includes a material selected from a group consisting of a nitride and a hydrogen and carbon containing silicon oxide.

16. The semiconductor device of claim 12, wherein at least a portion of the plurality of support structures is interconnected with unremoved portions of the dielectric layer.

17. The method of claim 16, further comprising at least one dielectric layer below the conductive bond pad having a Young's modulus less than approximately 30 Giga Pascals.

18. . The semiconductor device of claim 12, further comprising a barrier layer between the capping layer and the conductive bond pad.

19. The semiconductor device of claim 12, wherein the barrier layer includes a material selected from a group consisting of tantalum, titanium, tungsten, and chromium.

20. The semiconductor device of claim 12, wherein the conductive capping layer includes aluminum.

21. The semiconductor device of claim 12, wherein the conductive capping layer includes a material selected from the group consisting of nickel and palladium.

22. The semiconductor device of claim 12, further comprising a wirebond attached to the conductive capping layer.

23. The semiconductor device of claim 12, further comprising a conductive bump electrically connected to the conductive capping layer.